# THERMAL CYCLING EFFECTS ON A JPL FLIP CHIP PRINTED CIRCUIT BOARD

### Test Report

Richard Patterson NASA Glenn Research Center

&

Ahmad Hammoud QSS Group, Inc.

NASA Glenn Research Center Cleveland, Ohio

June 15, 2002

## THERMAL CYCLING EFFECTS ON A JPL FLIP CHIP PRINTED CIRCUIT BOARD

#### **Background**

Printed circuit boards employing flip chip technology are finding wide spread use in many industrial and aerospace applications. NASA is currently exploiting the use of such boards in electronic systems designed for future space missions. In addition to being lightweight and efficient, the boards must be able to withstand operation in harsh environments. These include severe temperature swings that are typically experienced in planetary exploration and deep space probes.

In a collaborative effort between NASA GRC and JPL under the NASA Electronic Parts and Packaging (NEPP) Program, a flip chip printed circuit board was provided by JPL for in-house evaluation under thermal cycling to extreme temperatures. The Flipchip Technologies, Inc. board (FB250/500 REV-A) was populated with a total of ten chips and had a 20-connector termination. A photograph of the flip chip printed circuit board is shown in Figures 1. The effect of thermal cycling on the board's electrical continuity and physical integrity was investigated.

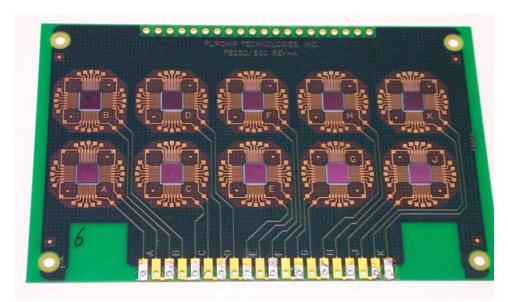


Figure 1. Top view of the flip chip printed circuit board.

#### **Test Procedure and Setup**

The flip chip board was characterized in terms of electrical continuity of the various circuit traces between the connector terminals 1 through 20. The board was examined for physical integrity and condition prior to any testing. Then resistance measurements were made in the temperature range of +90 °C to -125 °C. The printed circuit board was checked again for changes in physical integrity, such as delamination, warping, and discoloration. Next, the board was subjected to thermal cycling for a total of 10 cycles between +90 °C and -125 °C. A temperature rate of change of 10 °C/min was used throughout the cycling activity with a soak time of 10 minutes allowed at the extreme temperatures. After completion of the thermal cycling, the board was evaluated again in terms of electrical continuity (a resistance measurement) and structural integrity. The electrical continuity/resistance tests were performed using a Keithly 237 Source Measure Unit and an HP 34970A data acquisition/switching unit.

1

NASA GRC 6/02

#### **Test Results**

Changes in the resistance, i.e. trace continuity, between terminals 1 and 2 before the thermal cycling is shown in Figure 2 as a function of temperature. It can be clearly seen that the resistance changes in direct proportion to the test temperature. Figure 2 shows the same effect experienced by the trace resistance between terminals 19 and 20. In fact, such was the case for all the traces as depicted in table I. No visible damage was observed to the board due this temperature exposure.

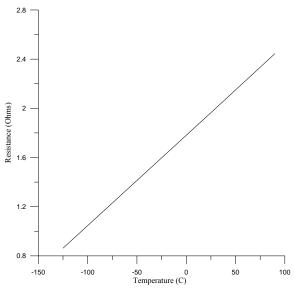


Figure 2. Resistance between terminals 1 and 2 versus temperature before thermal cycling.

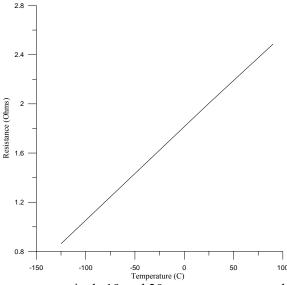


Figure 3. Resistance between terminals 19 and 20 versus temperature before thermal cycling.

Table I. Trace resistance before thermal cycling.

	Resistance $(\Omega)$ between terminals									
Temp (°C)	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	17-18	19-20
90	2.445	2.525	2.525	2.585	2.465	2.445	2.345	2.425	2.365	2.485
25	1.964	2.024	2.004	2.084	1.964	2.004	1.804	2.004	1.804	2.004
-125	.862	.842	.882	.902	.862	.862	.822	.842	.842	.862

2 NASA GRC 6/02

Figure 4 depicts the variation in the resistance between terminals 1 and 2 following the thermal cycling. It is evident that this limited cycling had little effect on the resistance (continuity) of this trace as the data did not change from that of pre-cycling condition, as was shown in Figure 2. Similarly, the circuit trace between terminals 19 and 20 did not exhibit any changes with cycling as depicted in Figure 5. Needless to say, all the other traces displayed the same behavior as can be seen from the data listed in Table II. Following the thermal cycling, the printed circuit board appeared to undergo no changes in its structural integrity as no delamination or warping was revealed upon examination visually or under a microscope.

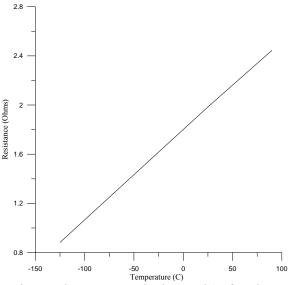


Figure 4. Resistance between terminals 1 and 2 after thermal cycling.

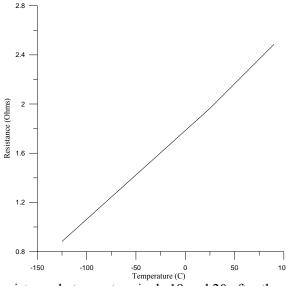


Figure 5. Resistance between terminals 19 and 20 after thermal cycling.

Table II. Trace resistance after thermal cycling.

	j 6									
	Resistance $(\Omega)$ between terminals									
Temp (°C)	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16	17-18	19-20
90	2.445	2.525	2.525	2.605	2.465	2.425	2.345	2.425	2.365	2.485
25	1.984	2.044	2.024	2.104	1.964	1.964	1.924	1.944	1.924	1.964
-125	.882	.902	.882	.922	.862	.862	.822	.862	.822	.882

Conclusion

A flip chip printed circuit board was evaluated under extreme temperatures between +90 °C to -125 °C. The Flipchip Technologies, Inc. board was populated with a total of ten chips and had a 20-connector termination. The effect of thermal cycling on the board's electrical continuity and physical integrity was also investigated. The results obtained indicate that this limited thermal cycling produced no effect on either the physical integrity or the electrical continuity of the board. Long term thermal cycling and aging as well as comprehensive testing are required to fully understand the behavior of this flip chip and other printed circuit boards under multi-stress conditions to determine their suitability for use in extreme temperature environments.

#### Acknowledgments

This work was performed under the NASA Glenn Research Center GESS Contract # NAS3-00145 and the NASA Electronic Parts and Packaging (NEPP) Program, Task "Interconnect Reliability of Cold Electronics".

4

NASA GRC 6/02